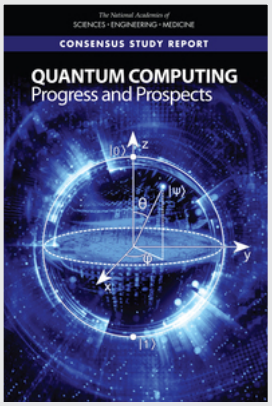

Quantum Computing: Progress and Prospects (2019)

DETAILS

272 pages | 6 x 9 | PAPERBACK
ISBN 978-0-309-47969-1 | DOI 10.17226/25196

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SUGGESTED CITATION

National Academies of Sciences, Engineering, and Medicine 2019. *Quantum Computing: Progress and Prospects*. Washington, DC: The National Academies Press. https://doi.org/10.17226/25196.

5

Essential Hardware Components of a Quantum Computer

Having shown in the prior chapters the potential of quantum computing, this chapter focuses on the hardware, and Chapter 6 explores the software needed to implement these computational processes and capabilities in practice. Quantum hardware is an active area of research. More than 100 academic groups and government-affiliate laboratories worldwide are researching how to design, build, and control qubit systems, and numerous established and start-up companies are now working to commercialize quantum computers built from superconducting and trapped ion qubits.

Even although reports in the popular press tend to focus on development of qubits and the number of qubits in the current prototypical quantum computing chip, any quantum computer requires an integrated hardware approach using significant conventional hardware to enable qubits to be controlled, programmed, and read out. The next section divides this hardware by its functions, creating the four hardware layers every quantum computer contains, and describes the expected relationship between classical and quantum computing resources.

Finding: While much progress has been made in the development of small-scale quantum computers, a design for a quantum computer that can scale to the size needed to break current cryptography has not been demonstrated, nor can it be achieved by straightforward scaling of any of the current implementations.

As a result, it is not clear whether the current leading quantum technologies will be used to create this class of machines. To provide a sense of the capability and challenges of different approaches, this chapter describes the quantum technologies currently being used to create early demonstration systems—that is, trapped ion and superconducting qubits—and their scaling issues, while also highlighting other promising qubit technologies that are currently less developed.

5.1 HARDWARE STRUCTURE OF A QUANTUM COMPUTER

Since a quantum computer must eventually interface with users, data, and networks—tasks that conventional computing excels at—a quantum computer can leverage a conventional computer for these tasks whenever it is most efficient to do so. Furthermore, qubit systems require carefully orchestrated control in order to function in a useful way; this control can be managed using conventional computers.

To assist in conceptualizing the necessary hardware components for an analog or gate-based quantum computer, the hardware can be modeled in four abstract layers: the "quantum data plane," where the qubits reside; the "control and measurement plane," responsible for carrying out operations and measurements on the qubits as required; the "control processor plane," which determines the sequence of operations and measurements that the algorithm requires, potentially using measurement outcomes to inform subsequent quantum operations; and the "host processor," a classical computer that handles access to networks, large storage arrays, and user interfaces. This host processor runs a conventional operating system/user interface, which facilitates user interactions, and has a high bandwidth connection to the control processor.

5.1.1 Quantum Data Plane

The quantum data plane is the "heart" of a QC. It includes the physical qubits and the structures needed to hold them in place. It also must contain any support circuitry needed to measure the qubits' state and perform gate operations on the physical qubits for a gate-based system or control the Hamiltonian for an analog computer. Control signals routed to the selected qubit(s) set the Hamiltonian it sees, which control the gate operation for a digital quantum computer. For gate-based systems, since some qubit operations require two qubits, the quantum data plane must provide a programmable "wiring" network that enables two or more qubits to interact. Analog systems often require richer communication between the qubits, which must be supported by this layer. As discussed in Chapter 2, high qubit fidelity requires strong isolation from the

environment, which has the effect of limiting connectivity—it may not be possible for every qubit to interact directly with every other qubit—so the computation needs to be mapped to the specific architectural constraints of this layer. These constraints mean that both the operation fidelity and connectivity are important metrics of the quantum data layer.[1]

Unlike a classical computer, where both the control plane and the data plane components use the same silicon technology and are integrated on the same device, control of the quantum data plane requires technology different from that of the qubits,[2] and is done externally by a separate control and measurement layer (described next). Control information for the qubits, which is analog in nature, must be sent to the correct qubit (or qubits). In some systems, this control information is transmitted electrically using wires, so these wires are part of the quantum data plane; in others, it is transmitted with optical or microwave radiation. Transmission must be implemented in a manner that has high specificity, so it affects only the desired qubit(s), without disrupting the other qubits in the system. This becomes increasingly difficult as the number of qubits grows; the number of qubits in a single module is therefore another important parameter of a quantum data layer.

Finding: The key properties that define the quality of a quantum data plane are the error rate of the single-qubit and two-qubit gates, the inter-qubit connectivity, qubit coherence times, and the number of qubits that may be contained within a single module.

5.1.2 Control and Measurement Plane

The control and measurement plane converts the control processor's digital signals, which indicates what quantum operations are to be performed, to the analog control signals needed to perform the operations on the qubits in the quantum data plane. It also converts the analog output of measurements of qubits in the data plane to classical binary data that the

[1] In some ways, the quantum data plane looks similar to a field programmable gate array, or FPGA. These are classical computing devices that contain a large number of flexible logic blocks. Each logic block can be configured—at program run time—to perform a logical function. In addition to these logic blocks, there is a configurable set of wires on the integrated circuit (IC), and one can configure the wires to interconnect the logic blocks to each other. This ability to program both the function of each logic block and their interconnection allows one to "program" the FPGA to implement the logic circuit needed to compute the desired result. Like an FPGA, "programming" of the quantum data plane also sets the function and the connections of the quantum computation.

[2] One potential qubit technology, semiconductor electrically gated qubits (see Section D.3.2) could be built using silicon, but even here it is not clear whether the processing for classical logic would be compatible with that required for qubit fabrication.

control processor can handle. The generation and transmission of control signals is challenging because of the analog nature of quantum gates; small errors in control signals, or irregularities in the physical design of the qubit, will affect the results of operations.[3] The errors associated with each gate operation accumulate as the machine runs.

Any imperfection in the isolation of these signals (so-called signal crosstalk) will cause small control signals to appear for qubits that should not otherwise be addressed during an operation, leading to small errors in their qubit state.[4] Proper shielding of the control signals is complicated by the fact that they must be fed through the apparatus which isolates the quantum date plane from its environment by vacuum, cooling, or both; this requirement constrains the type of isolation methods which are possible.

Fortunately, both qubit manufacturing errors and signal crosstalk errors are systematic, and change slowly with the mechanical configuration of the system. Effects of these slowly changing errors can be minimized by using control pulse shapes that reduce dependence of the qubit on these factors (see Section 3.2.1), and through periodic[5] system calibration, provided there is a mechanism to measure these errors and software to adjust the control signals to drive these errors to zero (system calibration). Since every control signal can potentially interact with every other control signal, the number of measurements and computation required to achieve this calibration more than doubles as the number of qubits in the system doubles.

The nature of a QC's control signals depends on the underlying qubit technology. For example, systems using trapped ion qubits usually rely upon microwave or optical signals (forms of electromagnetic radiation) transmitted through free space or waveguides and delivered to the location of the qubits. Superconducting qubit systems are controlled using microwave and low-frequency electrical signals, both of which are communicated through wires that run into a cooling apparatus (including a "dilution refrigerator" and a "cryostat") to reach the qubits inside the controlled environment.

Unlike classical gates, which have noise immunity and negligible error rates, quantum operations depend upon the precision with which control signals are delivered, and have nonnegligible error rates. Obtaining this

[3] Qubits that leverage basic atomic structure are not themselves subject to manufacturing variations. Instead, variations in the manufactured structures that hold these atoms, or in the manufactured systems generating the control signals, may lead to errors.

[4] It is worth noting that crosstalk can occur directly between the qubits themselves in the quantum data plane.

[5] The frequency of the calibration depends on the stability of both the quantum data plane and the control and measurement layer.

precision currently requires sophisticated generators built using classical technologies.

Since no quantum gate can be faster than the control pulse that implements it, even if the quantum system in principle allows ultrafast operation, the gate speed will be limited by the time required to construct and transmit an exquisitely precise control pulse. Fortunately, the speed of today's silicon technology is fast enough that gate speed is limited by the quantum data plane, and not the control and measurement plane. This gate speed is currently tens to hundreds of nanoseconds for superconducting qubits and one to a hundred microseconds for trapped ion qubits.

Finding: The speed of a quantum computer can never be faster than the time required to create the precise control signals needed to perform quantum operations.

5.1.3 Control Processor Plane and Host Processor

The control processor plane identifies and triggers the proper Hamiltonian or sequence of quantum gate operations and measurements (which are subsequently carried out by the control and measurement plane on the quantum data plane). These sequences execute the program, provided by the host processor, for implementing a quantum algorithm. Programs must be customized for the specific capabilities of the quantum layer by the software tool stack, as discussed in Chapter 6.

One of the most important and challenging tasks of the control processor plane will be to run the quantum error correction algorithm (if the QC is error corrected). Significant classical information processing is required to compute the quantum operations needed to correct errors based upon the measured syndrome results, and the time required for this processing may slow the operation of the quantum computer. This overhead is minimized if the error correction operations can be computed in a time comparable to that required for the quantum operations and measurements. Since this computational task grows with the size of the machine (the inputs and outputs of the function scale with the number of qubits, and the complexity scales with the "distance" of the error-correcting code), it is likely that this control processor plane will consist of multiple interconnected processing elements to handle the computational load.

Building a control processor plane for large quantum machines is challenging, and an active area of research. One approach splits the plane into two parts. The first part is simply a classical processor, which "runs" the quantum program. The second part is a scalable custom hardware

block[6] that directly interfaces with the control and measurement plane, and combines the higher level "instructions" output by the main controller with the syndrome measurements to compute the next operations to be performed on the qubits. The challenge is in creating scalable custom hardware that is fast enough and can scale with machine size, and in creating the right high-level instruction abstraction.

The control processor plane operates at a low level of abstraction: it converts compiled code to commands for the control and measurement layer. As a result, a user will not interact with (or need to understand) the control processor plane directly. Rather, the user will interact with a host computer. This plane will attach to that computer and act to accelerate the execution of some applications. This type of architecture is widely used in today's computers, with "accelerators" for everything from graphics to machine learning to networking. Such accelerators generally have a high-bandwidth connection to the host processor, usually through shared access to part of the host processor's memory, which can be used to transfer both the program the control processor should run, and the data it should use during the run.

The host processor is a classical computer, running a conventional operating system with standard supporting libraries for its own operation. This computing system provides all of the software development tools and services users expect from a computer system. It will run the software development tools necessary to create applications to be run on the control processor, which are different from those used to control today's classical computers, as well as provide storage and networking services that a quantum application might require while running. Attaching a quantum processor to a classical computer allows it to utilize all of its features without needing to start entirely from scratch.

5.1.4 Qubit Technologies

After the discovery of Shor's algorithm in 1994, serious efforts were launched to find an adequate physical system in which to implement quantum logic operations. The rest of this chapter reviews the current candidate qubit technology choices upon which to base a quantum computer. For the two furthest developed quantum technologies, superconducting and trapped ion qubits, this discussion includes details of the qubit and control planes in use in prototypical computers at the time of publication of this report (2018), the current challenges that must be overcome for each technology, and an assessment of the prospects for scale-up to very

[6] This layer could be built using FPGAs initially, and move to a custom integrated circuit later, if additional performance is required.

large processor sizes in the long term. The review of other emerging technologies provides a sense of their current status, and potential advantages if they are developed further.

5.2 TRAPPED ION QUBITS

The first quantum logic gate was demonstrated in 1995 using trapped atomic ions [1], following a theoretical proposal earlier in the same year [2]. Since the original demonstration, technical advances in qubit control have enabled experimental demonstration of fully functional processors at small scale and implementation of a wide range of simple quantum algorithms.

Despite success in small-scale demonstrations, the task of constructing scalable and quantum computers considered viable by current computing industry standards out of trapped ions remains a significant challenge. Unlike the very large scale integration (VLSI) of transistors enabled by the integrated circuit (IC), building a quantum computer based upon trapped ion qubits requires integration of technologies from a wide range of domains, including vacuum, laser, and optical systems, radio frequency (RF) and microwave technology, and coherent electronic controllers [3-5]. A path to a viable quantum computer must address these integration challenges.

A trapped ion quantum data plane comprises the ions that serve as qubits and a trap that holds them in specific locations. The control and measurement plane includes a very precise laser (or microwave) source that can be directed at a specific ion to affect its quantum state, another laser to "cool" and enable measurement of the ions, and a set of photon detectors to "measure" the state of the ions by detecting the photons that they scatter. Appendix B provides a technical overview of current strategies for constructing a trapped ion quantum data plane and its associated control and measurement plane.

5.2.1 Current Trapped Ion Quantum "Computers"

Based on the high-fidelity component operations demonstrated to date, small-scale ion trap systems have been assembled where a universal set of quantum logic operations can be implemented on a 5-20 qubit system in a programmable manner [6-9], forming the basis of a general-purpose quantum computer. Not surprisingly, at 2-5 percent for two-qubit gates, the error rates of individual quantum logic operations in these fully functional 5-20 qubit systems lag behind the 10^{-2} to 10^{-3} range [10,11] for state-of-the-art demonstrations of two-qubit systems, pointing to the challenge of maintaining the high fidelity across all qubits as the system

grows in size. Nonetheless, the versatility of these prototype systems has enabled a variety of quantum algorithms and tasks to be implemented on them. Fully programmable small-scale (three to seven qubit) trapped ion systems have been used to implement Grover's search algorithm [12,13], Shor's factoring algorithm [14], quantum Fourier transform [15,16], and others.

All of the prototype general-purpose trapped-ion quantum computer systems demonstrated to date consist of a chain of 5 to 20 static ions in a single potential well. In these machines, each single qubit gate operation takes 0.1-5 μs, and a multiqubit gate operation takes 50-3,000 μs depending on the nature of the gates used. Each ion in the chain interacts with every other ion in the chain due to the strong Coulomb interaction in a tight trap through motional degree of freedom that is shared among the ions. This interaction can be leveraged to realize quantum logic gates between nonadjacent ions, leading to dense connectivity among the qubits in a single ion chain. In one approach, a global entangling gate is applied to all qubits in the chain, where a subset of qubits are "hidden" from the others by changing their internal states, rendering them insensitive to the motion [17,18]. An alternative approach is to induce a two-qubit gate between an arbitrary pair of ions in the chain by illuminating specific ions with tightly focused and carefully tailored control signals, such that only the desired ions move—many control signals are used to make the force on all the other ions cancel out [19]. Using either approach, one can realize a general-purpose quantum processor with fully connected qubits [20], meaning that two-qubit gates may be implemented between arbitrary pairs of qubits in the system [21]; these capabilities are expected to scale to over 50 qubits in a relatively straightforward way [22].

5.2.2 Challenges and Opportunities for Creating a Scalable Ion Trap Quantum Computer

It is likely that some early, small-scale quantum computers (20-100 qubits) based on ion traps will become available by the early 2020s. Like current machines, these early demonstration systems are likely to consist of a single chain of ions and feature unique all-to-all connectivity among the qubits in the chain, efficiently implementing any quantum circuit with arbitrary circuit structures. However, many conceptual and technical challenges remain toward a creating a truly scalable, fault-tolerant ion trap quantum computer. Examples of such challenges include the difficulty of isolating individual ion motions as chain length increases, the number of ions one can individually address with gate laser beams, and measuring individual qubits. Further scaling of trapped ion quantum computers to well beyond the sizes necessary for demonstrating quantum supremacy

toward implementing small instances of useful quantum algorithms will require strategies beyond the single ion chain approach.

A first strategy for scaling beyond a single chain is to trap multiple chains of ions in a single chip with the capability to separate, move or "shuttle," and remerge one or more ions from one chain to another [23]. Such shuttling requires a complex trap with multiple controllable electrodes. Because the quantum information is stored in the internal states of the ion, which have been shown to be unaffected by shuttling between chains in small experiments, this approach does not contribute to any detectable decoherence [24]. Recent adoption of semiconductor microfabrication techniques has enabled the design and construction of highly complex ion traps, which are now routinely used for sophisticated shuttling procedures. This technology could potentially be used to connect multiple ion chains on a single chip, enabling for an increase in scale—provided that the controllers necessary to manipulate these qubits can be integrated accordingly. Even if this ion shuttling is successful on a single chip, eventually the system will need to be scaled up further. Two approaches are currently being explored: photonic interconnections, and tiling chips.

A strategy for connecting multiple qubit subsystems into a much larger system is to use quantum communication channels. One viable approach involves preparing one of the ions in a subsystem in a particular excited state and inducing it to emit a photon in such a way that the quantum state of the photon (for example, its polarization or frequency) is entangled with the ion qubit [25,26]. Two identical setups are used in the two subsystems to generate one photon from each ion, and the two photons can be interfered on a 50/50 beamsplitter and detected on the output ports of the beamsplitter. When both output ports simultaneously record detection of a photon [27], it signals that the two ions that generated the photons have been prepared in a maximally entangled state [28,29]. This protocol entangles a pair of ion qubits across two chips, without the ion qubits ever directly interacting with each other. Although the protocol must be attempted many times until it succeeds, its successful execution is heralded by an unmistakable signature (both detectors registering photons), and can be used deterministically in ensuing computational tasks—for example, to execute a two-qubit gate acting across chips [30]. This protocol was indeed demonstrated first in trapped ions [31] followed by other physical platforms [32-34]. Although the success rate of generating cross-chip entangled pairs in the early experiments was very low due the inefficiency of collecting and detecting the emitted photons (one successful event every ~1,000 seconds), dramatic improvements in the generation rate have been accomplished over the last few years (one successful event every ~200 ms) [35]. Given the continued improvement

of this technology, it might be possible that a cross-subsystem two-qubit gates could match the time scale of local two-qubit gates in a single chain (one event every ~100 μs) [36], making this a viable path to connecting ion trap chips using photonic networks. This approach opens up the possibility of using existing photonic networking technology, such as large optical cross-connect switches [37], to connect hundreds of ion trap subsystems into a network of modular, parallel quantum computers [38-40].

An alternative approach to the scaling beyond a single-ion trap chip is to tile all-electrical trap subsystems to create a system where ions from one ion trap chip can be transferred to another chip [41]. This shuttling across different integrated circuits requires careful alignment of shuttling channels and special preparation of the boundaries of these integrated circuits, which has not yet been demonstrated. In this proposal, all qubit gates are carried out by microwave fields and magnetic field gradients, free from the off-resonant spontaneous scattering and stability challenges associated with the use of laser beams [42]. While this integration approach remains entirely speculative at this point, this approach has the potential benefit of relying only on mature microwave technology and electrical control for the critical quantum logic gates, rather than using lasers and optics, which require much higher precision components.

For trapped ions, necessary technology developments toward scalable quantum computer systems include the ability to fabricate ion traps with higher levels of functionality, assemble stabilized laser systems with adequate control, deliver electromagnetic (EM) fields that drive the quantum gates (either microwave or optical) to the ions with sufficient levels of precision to affect only the qubit being targeted (preferably allowing multiple operations at a time), detect the qubit states in parallel without disturbing the data qubits, and program the control EM fields that manipulate the ion qubits so that the overall system achieves sufficient fidelity for the practical application needs. If these challenges are met, one will be able to take advantage of the strengths in trapped ions: some of the best performances of all physical systems in representing a single qubit, thanks to the fact that these qubits are fundamentally identical (as opposed to those which are manufactured), and the high fidelity of qubit operations at small experimental scales.

5.3 SUPERCONDUCTING QUBITS

Like current silicon integrated circuits, superconducting qubits are lithographically defined electronic circuits. When cooled to milli-Kelvin temperatures, they exhibit quantized energy levels (due to quantized states of electronic charge or magnetic flux, for example), and are thus sometimes called “artificial atoms” [43]. Their compatibility with

microwave control electronics, ability to operate at nanosecond time scales, continually improving coherence times, and potential to leverage lithographic scaling, all converge to place superconducting qubits among the forefront of the qubit modalities being considered for both digital quantum computation and quantum annealing. Appendix C provides a technical overview of current strategies for constructing a superconductor quantum data plane and its associated control and measurement plane.

5.3.1 Current Superconducting Quantum "Computers"

In the context of digital quantum computation and quantum simulations, the present state-of-art for operational gate error rate is better than (below) 0.1 percent for single-qubit gates [44-46] and 1 percent for two-qubit gates [47], below the error threshold for the most lenient error detection protocols—for example, the surface code. Based on these developments, superconducting qubit circuits with around 10 qubits have been engineered to demonstrate prototype quantum algorithms [48,49] and quantum simulations [50,51], prototype quantum error detection [52-55], and quantum memories [56], and, as of 2018, cloud-based 5-, 16-, and 20-qubit circuits are available to users worldwide. However, the error rates are higher in these larger machines—for example, the 5-qubit machines available on the Web in 2018 have gate error rates of around 5 percent [57,58].

In the context of quantum annealing, commercial systems exist with over 2,000 qubits and integrated cryogenic control based on classical superconducting circuitry [59,60]. These are the largest qubit-based systems currently available, with two orders of magnitude (100 times) more qubits than current gate-based QCs. To achieve this scale machine required careful design trade-offs and significant engineering effort. The decision to integrate the control electronics with the qubits enabled D-Wave to rapidly scale the number of qubits in their system, but also results in the qubits being built in a more lossy material. They purposely traded off qubit fidelity for an easier scaling path. Thus, the coherence times of the qubits in these machines are over 3 orders of magnitude worse than those in current gate-based machines, although this is expected to be less of a limitation for quantum annealers than for gate-based machines.

Progress in gate-based machines has emphasized the optimization of qubit and gate fidelities, at sizes limited to on the order of tens of qubits. Since the first demonstration of a superconducting qubit in 1999, the qubit coherence time T_2 in gate-level machines has improved more than five orders-of-magnitude, standing at around 100 microseconds today. This remarkable improvement in coherence arose from reducing energy losses in the qubit through advances in materials science, fabrication engineering, and qubit design by groups worldwide.

5.3.2 Challenges and Opportunities for Creating a Scalable Quantum Computer

The current approach, using room temperature control and measurement planes, with multiple wires per qubit, should scale to around 1,000 physical qubits [61]. This section reviews the factors that cause this limit, and then discusses what is currently known about the path to even larger machines.

Reaching Many Hundreds of Qubits

Many factors will limit the size of machine that can be achieved by simply scaling up the number of qubits placed on a single integrated circuit. These include the following:

- *Maintaining qubit quality while scaling up the number of bits.* Superconducting qubits are lithographically scalable and compatible with semiconductor fabrication tools [62]. High-coherence qubits have been demonstrated on 200-mm wafers in a research foundry environment. In scaling to larger numbers of qubits, one needs to at least maintain qubit coherence and, ideally, increase it, as larger systems will likely aim to solve larger problems that require additional time, and higher fidelity enables more operations to be performed during the coherence time of the quantum processor. Of course, the fabrication variation that a number of qubits spans gets worse as the number of qubits increases, since a larger number of cells will include more improbable variations. The current approach to fabricating high-fidelity tunable qubits—shadow evaporation—will likely scale to the level of thousands of qubits, based on the process monitoring of device yield and variations currently being implemented at places like the Massachusetts Institute of Technology Lincoln Laboratory. Today's nominally identical qubits vary in frequency with a sigma of around 150 MHz, corresponding to a sigma in the Josephson junction critical current of 2-3 percent. While sufficient for scaling tunable qubits to the 1,000-qubit level, certain fixed-frequency qubit schemes will not be able to handle this larger variation.
- *Refrigeration, wiring, and packaging.* Present dilution refrigerator technology can handle up to several thousand DC wires and coaxial cables, which should support around 1,000 qubits. Achieving this level of wiring requires proper materials to reduce thermal loads, in particular from 300 K to the 3 K stage, and miniaturized coaxes and connectors. While the bandwidth required for control is generally limited to around 12 GHz for qubits being designed

today, controlling the out-of-band impedance out to higher frequencies can be important to minimize decoherence, and becomes more difficult as the physical size increases.

Building a large-scale quantum computer will require two dimensional (2D) arrays of qubits, and areal connection from the qubits to their housing, or "package," and from the package to the wires fed through the cryostat. This areal connection will need three-dimensional (3D) integration schemes using flip-chip bump-bonding and superconducting through-silicon vias, technologies that are being developed to connect high-coherence qubit chips with multilayer interconnect routing wafers [63,64].

- *Control and measurement.* As mentioned earlier, present designs require per qubit control signal generation. While in many current machines, these signals are generated by standard lab equipment, several companies now provide rack-mounted card designs that should scale to a few thousand qubits. Using rack-mounted electronics means that any time the next operation depends on a prior measurement, a common operation in error correction algorithms, there will be a delay in the machine's operation. Sending a signal down, getting a signal back, inferring the next signal to send, and triggering it to be sent takes 500-1,000 ns using current equipment, and limits the ultimate clock speed of the quantum computer. While this should be sufficient for 1,000 qubit circuits, reducing the clock period is advantageous, as it translates directly to lower error rates.

Scaling to Larger-Size Machines

First, qubit fidelities need to be improved to provide the lower error rates needed to support practical quantum error correction. Materials, fabrication and circuit-design advances will be key to achieving 10^{-3} to 10^{-4} qubit error rates. In addition, as the size of the computer increases to millions of qubits and beyond, advanced process monitoring, statistical process control, and new methods for reducing defects relevant to high-coherence devices will be required to assess and improve qubit yield. Just as fabrication tools have been specialized to target specific, advanced complementary metal-oxide semiconductor (CMOS) processes, it is likely that specialized tools that target specific qubit-fabrication processes will need to be developed to enhance yield and minimize fabrication-induced defects that cause decoherence.

Wafer real estate is another consideration for larger machines. Assuming qubit unit cells with repeat distance critical dimensions of 50 microns (state-of-the-art today) [65], a large integrated circuit of 20 mm by 20 mm

could contain around 1,600 qubits. If one used an entire 300 mm wafer for one processor, the wafer could hold around 250,000 qubits. While that is sufficient for the near future, reducing the qubit unit cell critical dimension while retaining coherence and controllability will increase qubit density and enable larger numbers of qubits on a single 300 mm wafer.

Moving to wafer-size integrated circuits requires creating a new package. Today's high-coherence qubits operate in pristine microwave environments. The qubits are generally around 5 GHz, which corresponds to a free-space wavelength of around 60 mm. The wavelength is further reduced in the presence of dielectrics like the silicon wafer. Using the rule of thumb that a clean microwave environment requires dimensions less than one-quarter of a wavelength, it is clear that further research is needed before large high-quality packages can be built.

Controlling more than a thousand qubits will require a new strategy for the control and measurement plane. Instead of externally driving each control signal, some logic/control closer to the qubit will drive these signals, and a smaller number of external signals will be used to control this logic. This control logic will need to be introduced using either 3D integration to connect the qubit plane with this local control plane or fabricated monolithically (but must be done so without compromising qubit coherence and gate fidelity). Of course, this means that this logic will operate at very cold temperatures, either at tens of milli-Kelvins, or at 4 K. Operating at 4 K is much easier, since the capacity for heat dissipation is larger, and it saves on the wire count from room temperature to 4 K, but it still requires extensive control wiring to continue down to the base-temperature stage in the cryostat. While there are technologies that could operate at these temperatures, including cryogenic CMOS, single-flux quantum (SFQ), reciprocal quantum logic (RQL), and adiabatic quantum flux parametrons, significant research will be needed to be create these designs at scale, and then determine which approaches are able to create a local control and measurement layer that supports the needed high-fidelity qubit operations.

Even if one is able to scale to 300 mm wafers, a large quantum computer will need to use a number of these subsystems, and with high probability, the optimal size of the subsystem will be modules smaller than that. Thus, there will be a need to connect these subsystems to each other with some kind of quantum interconnect. There are two general approaches that are currently being pursued. One assumes that the interconnection between the modules is at milli-Kelvin temperatures, so one can use microwave photons to communicate. This involves creating guided channels for these photons, interconverting quantum information between a qubit and a microwave photon, and then converting the quantum information back from that photon to a second, distant qubit.

The other option is to couple the qubit state to a higher energy optical photon, which requires a high-fidelity microwave-to-optical conversion technique. This is an area of active research today.

5.4 OTHER TECHNOLOGIES

Since many technical challenges remain in scaling either trapped ion or superconducting quantum computers, a number of research groups are continuing to explore other approaches for creating qubits and quantum computers. These technologies are much less developed, and are still focused on creating single qubit and two qubit gates. Appendix D provides an introduction to these approaches, which is summarized in this section.

Photons have a number of properties that make them an attractive technology for quantum computers: they are quantum particles that interact weakly with their environment and with each other. This natural isolation from the environment makes them an obvious approach to quantum communication. This base communication utility, combined with excellent single-qubit gates with high fidelity means that many early quantum experiments were done using photons. One key challenge with photonic quantum computers is how to create robust two-qubit gates. Researchers are currently working on two approaches for this issue. In linear optics quantum computing, an effective strong interaction is created by a combination of single-photon operations and measurements, which can be used to implement a probabilistic two-qubit gate, which heralds when it was successful. A second approach uses small structures in semiconductor crystals for photon interaction, and can also be considered a type of semiconductor quantum computer. These structures can be naturally occurring, called "optically active defects," or man-made, which are often a structure called a "quantum dot."

Work on building small-scale linear photon computers has been successful, and there are a number of groups trying to scale up the size of these machines. One key scaling issue for these machines is the "size" of a photonic qubit. Because the photons used in photonic quantum computing typically have wavelengths that are around a micron, and because the photons move at the speed of light and are typically routed along one dimension of the optical chip, increasing the number of photons, and hence the number of qubits, to extremely large numbers in a photonic device is even more challenging than it is in systems with qubits that can be localized in space. However, arrays with many thousands of qubits are expected to be possible [66].

Neutral atoms are another approach for qubits that is very similar to trapped ions, but instead of using ionized atoms and exploiting their charge to hold the qubits in place, neutral atoms and laser tweezers are

used. Like trapped ion qubits, optical and microwave pulses are used for qubit manipulation, with lasers also being used to cool the atoms before computation. In 2018, systems with 50 atoms have been demonstrated with relatively compact spacing between the atoms [67]. These systems have been used as analog quantum computers, where the interactions between qubits can be controlled by adjusting the spacing between the atoms. Building gate-based quantum computers using this technology requires creating high-quality two-qubit operations and isolating these operations from other neighboring qubits. As of mid-2018, entanglement error rates of 3 percent have been achieved in isolated two-qubit systems [68]. Scaling up a gate-based neutral atom system requires addressing many of the same issues that arise when scaling a trapped ion computer, since the control and measurement layers are the same. Its unique feature compared to trapped ions is its potential for building multidimensional arrays.

Semiconductor qubits can be divided into two types depending on whether they use photons or electrical signals to control qubits and their interactions. Optically gated semiconductor qubits typically use optically active defects or quantum dots that induce strong effective couplings between photons, while electrically gated semiconductor qubits use voltages applied to lithographically defined metal gates to confine and manipulate the electrons that form the qubits. While less developed than other quantum technologies, this approach is more similar to that used for current classical electronics, potentially enabling the large investments that have enabled the tremendous scalability of classical electronics to facilitate the scaling of quantum information processors. Scaling optically gated qubits requires improved uniformity and requires accommodation of the need to individually address optically each qubit. Electrically gated qubits are potentially very dense, but material issues have limited the quality of even single-qubit gates until recently [69]. While high density may enable a very large number of qubits to be integrated on the chip, it exacerbates the problem of building a control and measurement plane for these types of qubits: providing the needed wiring while avoiding interference and crosstalk between control signals will be extremely challenging.

The final approach to quantum computing discussed here uses topological qubits. In this system, operations on the physical qubits have extremely high fidelities because the qubit operations are protected by topological symmetry implemented at the microscopic level: error correction is done by the qubit itself. This will reduce and possibly eliminate the overhead of performing explicit quantum error correction. While this would be an amazing advance, topological qubits are the least developed technology platform. In mid-2018, there are many nontrivial steps

that need to be done to demonstrate the existence of a topological qubit, including experimentally observing the basic structure that underlies these qubits. Once these structures are built and controlled in the lab, the error resilience properties of this approach might enable it to scale faster than the other approaches.

5.5 FUTURE OUTLOOK

Many qubit technologies have significantly improved over the past decade, leading to the small gate-based quantum computers available today. For all qubit technologies, the first major challenge is to lower qubit error rates in large systems while enabling measurements to be interspersed with qubit operations. As mentioned in Chapter 3, the surface code is currently the primary approach to error correction for systems with high error rates. Current systems are limited by two-qubit gate error rates, which is still above the surface code threshold for the larger systems available today; error rates of at least an order of magnitude better than threshold are required if quantum error correction is to be practical.

At ~1,000 physical qubits—used for both data qubits and syndrome measurement qubits—one can implement a distance ~16 quantum error correcting code for a single logical qubit. Assuming a physical-qubit error rate of 10^{-3} (an arbitrary but reasonable estimate, more than 10 times better than currently reported for 10 to 20 qubit machines), one can achieve a logical error rate of approximately 10^{-10}. Improving the physical error rate to 10^{-4} would decrease the logical error rate to 10^{-18}. This example illustrates the substantial win in overall logical error rate (from 10^{-10} to 10^{-18}, eight orders of magnitude) by a relatively modest improvement in physical qubit error rate (from 10^{-3} to 10^{-4}, only one order of magnitude). Clearly, improving physical qubit fidelity—through improvements to fabrication and control—is paramount to demonstrating logical qubits or even a machine with physical qubits that can cascade an interesting number of qubit operations before losing coherence.

The next challenge is to increase the number of qubits in the quantum computer. It seems clear that one will be able to build ICs with hundreds of superconductor qubits in the near future using procedures very similar to the methods used for today's 20-qubit ICs. In fact, by mid-2018 a number of companies have announced ICs that contained order of 50 qubits, but as of this writing there are no published results benchmarking the functionality or error rates of these systems. Unlike conventional silicon scaling, where creating the manufacturing process for the more complex integrated circuit set the pace of scaling, for quantum computing, scaling will be dictated by the degree of difficulty in obtaining low error rates with these larger qubit systems, a task that requires joint optimization

of the IC, package, control and measurement plane, and the calibration method used.

Scaling trapped ion computing requires the design of new trap systems and the control and measurement plane optics/electronics for these new traps. The next generation are likely to use linear ion traps, which will scale to the order of 100 qubits. Further scaling will require another change to the trap design to enable shuttling of ions between different groups, which should also allow more flexible qubit measurements.

At some point in increasing the number of qubits in a quantum processor or chip, the scaling will become easier using a modular approach, where a number of chips are linked together to create a larger machine rather than creating a larger chip. A modular design will require the development of a fast, low error rate quantum interconnection between the modules; with photonic connections the most promising due to their speed and fidelity. While the component technologies and baseline protocols for realizing some of these integration strategies have already been demonstrated, system-scale demonstration with practical levels of performance remains a major challenge.

As a result of the challenges facing superconducting and trapped ion quantum data planes, it is not yet clear if or when either of these technologies can scale to the level needed for a large error corrected quantum computer. Thus, at this time, the viability of other, currently less-developed quantum data plane technologies cannot be ruled out, nor can the possibility that hybrid systems making use of multiple technologies might prevail.

5.6 NOTES

[1] C. Monroe, D.M. Meekhof, B.E. King, W.M. Itano, and D.J. Wineland, 1995, Demonstration of a fundamental quantum logic gate, *Physical Review Letters* 75:4714.

[2] J.I. Cirac and P. Zoller, 1995, Quantum computations with cold trapped ions, *Physical Review Letters* 74:4091.

[3] C. Monroe and J. Kim, 2013, Scaling the ion trap quantum processor, *Science* 339:1164-1169.

[4] K.R. Brown, J. Kim and C. Monroe, 2016, Co-designing a scalable quantum computer with trapped atomic ions, *npj Quantum Information* 2:16034.

[5] J. Kim, S. Crain, C. Fang, J. Joseph, and P. Maunz, 2017, "Enabling Trapped Ion Quantum Computing with MEMS Technology," pp. 1-2 in *2017 International Conference on Optical MEMS and Nanophotonics (OMN),* https://ieeexplore.ieee.org.

[6] D. Hanneke, J.P. Home, J.D. Jost, J.M. Amini, D. Leibfried and D.J. Wineland, 2010, Realization of a programmable two-qubit quantum processor, *Nature Physics* 6:13.

[7] P. Schindler, D. Nigg, T. Monz, J. Barreiro, E. Martinez, S. Wang, S. Quint, M. Brandl, V. Nebendahl, C. Roos, M. Chwalla, M. Hennrich, and R. Blatt, 2013, A quantum information processor with trapped ions, *New Journal of Physics* 15:123012.

[8] S. Debnath, N.M. Linke, C. Figgatt, K.A. Landsman, K. Wright, and C. Monroe, 2016, Demonstration of a small programmable quantum computer with atomic qubits, *Nature* 536:63-66.

[9] N. Friis, O. Marty, C. Maier, C. Hempel, M. Holzapfel, P. Jurcevic, M. Plenio, M. Huber, C. Roos, R. Blatt, and B. Lanyon, 2017, "Observation of Entangled States of a Fully Controlled 20 Qubit System," arXiv:1711.11092.

[10] J.P. Gaebler, T.R. Tan, Y. Lin, Y. Wan, R. Bowler, A.C. Keith, S. Glancy, K. Coakley, E. Knill, D. Leibfried, and D.J. Wineland, 2016, High-fidelity universal gate set for $^{9}Be^{+}$ ion qubits, *Physical Review Letters* 117:060505.

[11] C.J. Ballance, T.P. Harty, N.M. Linke, M.A. Sepiol, and D.M. Lucas, 2016, High-fidelity quantum logic gates using trapped-ion hyperfine qubits, *Physical Review Letters* 117:060504.

[12] K.-A. Brickman, P.C. Haljan, P.J. Lee, M. Acton, L. Deslauriers, and C. Monroe, 2005, Implementation of Grover's quantum search algorithm in a scalable system, *Physical Review A* 72:050306(R).

[13] C. Figgatt, D. Maslov, K.A. Landsman, N.M. Linke, S. Debnath, and C. Monroe, 2017, Complete 3-qubit grover search on a programmable quantum computer, *Nature Communications* 8:1918.

[14] T. Monz, D. Nigg, E.A. Martinez, M.F. Brandl, P. Schindler, R. Rines, S.X. Wang, I.L. Chuang, and R. Blatt, 2016, Realization of a scalable Shor algorithm, *Science* 351:1068-1070.

[15] J. Chiaverini, J. Britton, D. Leibfried, E. Knill, M.D. Barrett, R.B. Blakestad, W.M. Itano, J.D. Jost, C. Langer, R. Ozeri, T. Schaetz, and D.J. Wineland, 2005, Implementation of the semiclassical quantum Fourier transform in a scalable system, *Science* 308:997-1000.

[16] A. Sørensen and K. Mølmer, 1999, Quantum computation with ions in a thermal motion, *Physical Review Letters* 82:1971.

[17] B.P. Lanyon, C. Hempel, D. Nigg, M. Müller, R. Gerritsma, F. Zähringer, P. Schindler, J.T. Barreiro, M. Rambach, G. Kirchmair, M. Hennrich, P. Zoller, R. Blatt, and C.F. Roos, 2011, Universal digital quantum simulation with trapped ions, *Science* 334:57-61.

[18] P.C. Haljan, K.-A. Brickman, L. Deslauriers, P.J. Lee, and C. Monroe, 2005, Spin-dependent forces on trapped ions for phase-stable quantum gates and entangled states of spin and motion, *Physical Review Letters* 94:153602.

[19] S.-L. Zhu, C. Monroe, and L.-M. Duan, 2006, Arbitrary-speed quantum gates within large ion crystals through minimum control of laser beams, *Europhyics Letters* 73(4):485.

[20] C.J. Ballance, T.P. Harty, N.M. Linke, M.A. Sepiol, and D.M. Lucas, 2016, High-fidelity quantum logic gates using trapped-ion hyperfine qubits, *Physical Review Letters* 117:060504.

[21] N.M. Linke, D. Maslov, M. Roetteler, S. Debnath, C. Figgatt, K.A. Landsman, K. Wright, and C. Monroe, 2017, Experimental comparison of two quantum computing architectures, *Proceedings of the National Academy of Sciences of the U.S.A.* 114:13.

[22] J. Zhang, G. Pagano, P.W. Hess, A. Kyprianidis, P. Becker, H.B. Kaplan, A.V. Gorshkov, Z.-X. Gong, and C. Monroe, 2017, Observation of a many-body dynamical phase transition with a 53-qubit quantum simulator, *Nature* 551:601-604.

[23] J. Chiaverini, B.R. Blakestad, J.W. Britton, J.D. Jost, C. Langer, D.G. Leibfried, R. Ozeri, and D.J. Wineland, 2005, Surface-electrode architecture for ion-trap quantum information processing, *Quantum Information and Computation* 5:419.

[24] J. Kim, S. Pau, Z. Ma, H.R. McLellan, J.V. Gates, A. Kornblit, R.E. Slusher, R.M. Jopson, I. Kang, and M. Dinu, 2005, System design for large-scale ion trap quantum information processor, *Quantum Information and Computation* 5:515.

[25] L.-M. Duan, B.B. Blinov, D.L. Moehring, and C. Monroe, 2004, Scalable trapped ion quantum computation with a probabilistic ion-photon mapping, *Quantum Information and Computation* 4:165-173.

[26] B.B. Blinov, D.L. Moehring, L.-M. Duan and C. Monroe, 2004, Observation of a entanglement between a single trapped atom and a single photon, *Nature* 428:153-157.

[27] D. Bouwmeester, P. Jian-Wei, K. Mattle, M. Eibl, H. Weinfurter, and A. Zeilinger, 1997, Experimental quantum teleportation, *Nature* 390:575-579.
[28] C. Simon and W.T.M. Irvine, 2003, Robust long-distance entanglement and a loophole-free bell test with ions and photons, *Physical Review Letters* 91:110405.
[29] L.-M. Duan, M.J. Madsen, D.L. Moehring, P. Maunz, R.N. Kohn Jr., and C. Monroe, 2006, Probabilistic quantum gates between remote atoms through interference of optical frequency qubits, *Physical Review A* 73:062324.
[30] D. Gottesman and I. Chuang, 1999, Quantum teleportation is a universal computational primitive, *Nature* 402:390-393.
[31] D.L. Moehring, P. Maunz, S. Olmschenk, K.C. Younge, D.N. Matsukevich, L.-M. Duan, and C. Monroe, 2007, Entanglement of a single-atom quantum bits at a distance, *Nature* 449:68-71.
[32] J. Hofmann, M. Krug, N. Ortegel, L. Gérard, M. Weber, W. Rosenfeld, and H. Weinfurter, 2012, Heralded entanglement between widely separated atoms, *Science* 337:72-75.
[33] H. Bernien, B. Hensen, W. Pfaff, G. Koolstra, M.S. Blok, L. Robledo, T.H. Taminiau, M. Markham, D.J. Twitchen, L. Childress, and R. Hanson, 2013, Heralded entanglement between solid-state qubits separated by 3 meters, *Nature* 497:86-90.
[34] A. Delteil, Z. Sun, W. Gao, E. Togan, S. Faelt and A. Imamoğlu, 2015, Generation of heralded entanglement between distant hole spins, *Nature Physics* 12:218-223.
[35] D. Hucul, I.V. Inlek, G. Vittorini, C. Crocker, S. Debnath, S.M. Clark, and C. Monroe, 2015, Modular entanglement of atomic qubits using photons and phonons, *Nature Physics* 11:37-42.
[36] T. Kim, P. Maunz, and J. Kim, 2011, Efficient collection of single photons emitted from a trapped ion into a single-mode fiber for scalable quantum-information processing, *Physical Review A* 84:063423.
[37] J. Kim, C.J. Nuzman, B. Kumar, D.F. Lieuwen, J.S. Kraus, A. Weiss, C.P. Lichtenwalner, et al., 2003, "1100 × 1100 port MEMS-based optical crossconnect with 4-dB maximum loss," *IEEE Photonics Technology Letters* 15:1537-1539.
[38] P. Schindler, D. Nigg, T. Monz, J.T. Barreiro, E. Martinez, S.X. Wang, S. Quint, et al., 2013, A quantum information processor with trapped ions, *New Journal of Physics* 15:123012.
[39] D. Hanneke, J.P. Home, J.D. Jost, J.M. Amini, D. Leibfried, and D.J. Wineland, 2010, Realization of a programmable two-qubit quantum processor, *Nature Physics* 6:13-16.
[40] C. Monroe, R. Raussendorf, A. Ruthven, K.R. Brown, P. Maunz, L.-M. Duan, and J. Kim, 2014, Large-scale modular quantum-computer architecture with atomic memory and photonic interconnects, *Physical Review A* 89:022317.
[41] B. Lekitsch, S. Weidt, A.G. Fowler, K. Mølmer, S.J. Devitt, C. Wunderlich, and W.K. Hensinger, 2017, Blueprint for a microwave trapped ion quantum computer, *Science Advances* 3:e1601540.
[42] C. Piltz, T. Sriarunothai, S.S. Ivanov, S. Wölk and C. Wunderlich, 2016, Versatile microwave-driven trapped ion spin system for quantum information processing, *Science Advances* 2:e1600093.
[43] W.D. Oliver and P.B. Welander, 2013, Materials in superconducting quantum bits, *MRS Bulletin* 38(10):816-825.
[44] S. Gustavsson, O. Zwier, J. Bylander, F. Yan, F. Yoshihara, Y. Nakamura, T.P. Orlando, and W.D. Oliver, 2013, Improving quantum gate fidelities by using a qubit to measure microwave pulse distortions, *Physical Review Letters* 110:0405012.
[45] R. Barends, J. Kelly, A. Megrant, A. Veitia, D. Sank, E. Jeffrey, T.C. White, et al., 2014, Logic gates at the surface code threshold: Supercomputing qubits poised for fault-tolerant quantum computing, *Nature* 508:500-503.
[46] S. Sheldon, E. Magesan, J. Chow, and J.M. Gambetta, 2016, Procedures for systematically turning up cross-talk in the cross-resonance gate, *Physical Review A* 93:060302.

[47] R. Barends, J. Kelly, A. Megrant, A. Veitia, D. Sank, E. Jeffrey, T.C. White, et al., 2014, Superconducting quantum circuits at the surface code threshold for fault tolerance, *Nature* 508(7497):500.

[48] L. DiCarlo, J.M. Chow, J.M. Gambetta, L.S. Bishop, B.R. Johnson, D.I. Schuster, J. Majer, A. Blais, L. Frunzio, S.M. Girvin, and R.J. Schoelkopf, 2009, Demonstration of two-qubit algorithms with a superconducting quantum processor, *Nature* 460:240-244.

[49] E. Lucero, R. Barends, Y. Chen, J. Kelly, M. Mariantoni, A. Megrant, P. O'Malley, et al., 2012, Computing prime factors with a Josephson phase qubit quantum processor, *Nature Physics* 8:719-723.

[50] P.J.J. O'Malley, R. Babbush, I.D. Kivlichan, J. Romero, J.R. McClean, R. Barends, J. Kelly, et al., 2016, Scalable quantum simulation of molecular energies, *Physical Review X* 6:031007.

[51] N.K. Langford, R. Sagastizabal, M. Kounalakis, C. Dickel, A. Bruno, F. Luthi, D.J. Thoen, A. Endo, and L. DiCarlo, 2017, Experimentally simulating the dynamics of quantum light and matter at deep-strong coupling, *Nature Communications* 8:1715.

[52] M.D. Reed, L. DiCarlo, S.E. Nigg, L. Sun, L. Frunzio, S.M. Girvin, and R.J. Schoelkopf, 2012, Realization for three-qubit quantum error correction with superconducting circuits, *Nature* 482:382-385.

[53] J. Kelly, R. Barends, A.G. Fowler, A. Megrant, E. Jeffrey, T. C. White, D. Sank, et al., 2015, State preservation by repetitive error detection in a superconducting quantum circuit, *Nature* 519:66-69.

[54] A.D. Córcoles, E. Magesan, S.J. Srinivasan, A.W. Cross, M. Steffen, J.M. Gambetta, and J.M. Chow, 2015, Demonstration of a quantum error detection code using a square lattice of four superconducting qubits, *Nature Communications* 6:6979.

[55] D. Ristè, S. Poletto, M.-Z. Huang, A. Bruno, V. Vesterinen, O.-P. Saira, and L. DiCarlo, 2015, Detecting bit-flip errors in a logical qubit using stabilizer measurements, *Nature Communications* 6:6983.

[56] N. Ofek, A. Petrenko, R. Heeres, P. Reinhold, Z. Leghtas, B. Vlastakis, Y. Liu, et al., 2016, Extending the lifetime of a quantum bit with error correction in superconducting circuits, *Nature* 536:441-445.

[57] IBM Q Team, 2018, "IBM Q 5 Yorktown Backend Specification V1.1.0," https://ibm.biz/qiskit-yorktown; IBM Q Team, 2018, "IBM Q 5 Tenerife backend specification V1.1.0," https://ibm.biz/qiskit-tenerife.

[58] Ibid.

[59] M.W. Johnson, M.H.S. Amin, S. Gildert, T. Lanting, F. Hamze, N. Dickson, R. Harris, et al., 2011, Quantum annealing with manufactured spins, *Nature* 473:194-198.

[60] D Wave, "Technology Information," http://dwavesys.com/resources/publications.

[61] John Martinis, private conversation.

[62] W.D. Oliver and P.B. Welander, 2013, Materials in superconducting qubits, *MRS Bulletin* 38:816.

[63] D. Rosenberg, D.K. Kim, R. Das, D. Yost, S. Gustavsson, D. Hover, P. Krantz, et al., 2017, 3D integrated superconducting qubits, *npj Quantum Information* 3:42.

[64] B. Foxen, J.Y. Mutus, E. Lucero, R. Graff, A. Megrant, Y. Chen, C. Quintana, et al., 2017, "Qubit Compatible Superconducting Interconnects," arXiv:1708.04270.

[65] J.M. Chow, J.M. Gambetta, A.D. Co´rcoles, S.T. Merkel, J.A. Smolin, C. Rigetti, S. Poletto, G.A. Keefe, M.B. Rothwell, J.R. Rozen, M.B. Ketchen, and M. Steffen, 2012, Universal quantum gate set approaching fault-tolerant thresholds with superconducing qubits, *Physical Review Letters* 109:060501.

[66] See, for example, J.W. Silverstone, D. Bonneau, J.L. O'Brien, and M.G. Thompson, 2016, Silicon quantum photonics, *IEEE Journal of Selected Topics in Quantum Electronics* 22:390-402;

T. Rudolph, 2017, Why I am optimistic about the silicon-photonic route to quantum computing?, *APL Photonics* 2:030901.

[67] H. Bernien, S. Schwartz, A. Keesling, H. Levine, A. Omran, H. Pichler, S. Choi, A.S. Zibrov, M. Endres, M. Greiner, V. Vuletić, and M.D. Lukin, 2017, "Probing Many-Body Dynamics on a 51-Atom Quantum Simulator," preprint arXiv:1707.04344.

[68] H. Levine, A. Keesling, A. Omran, H. Bernien, S. Schwartz, A.S. Zibrov, M. Endres, M. Greiner, V. Vuletić, and M.D. Lukin, 2018, "High-Fidelity Control and Entanglement of Rydberg Atom Qubits," preprint arXiv:1806.04682.

[69] J.J. Pla, K.Y. Tan, J.P. Dehollain, W.H. Lim, J.J. Morton, D.N. Jamieson, A.S. Dzurak, and A. Morello, 2012, A single-atom electron spin qubit in silicon, *Nature* 489:541-545.